

TITLE: AN ELECTRONIC DEVICE COMPRISING ENHANCEMENT MODE PHEMT DEVICES, DEPLETION MODE PHEMT DEVICES, AND POWER PHEMT DEVICES ON A SINGLE SUBSTRATE AND METHOD OF CREATION

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FIELD OF THE INVENTION

[0001] The present invention relates to integrated circuits, especially those capable of operating at high frequencies.

BACKGROUND OF THE INVENTION

[0002] Numerous integrated circuits have been proposed and fabricated over the years. As devices gain faster clock speeds, a need has arisen for integrated circuits that possess the ability to function at high clock speeds with appropriate power consumption and power generation.

[0003] Some circuits, e.g. analog/digital converters, typically operate at lower frequencies as the typical method of constructing such circuits involves using printed wiring boards which can limit the functional processing speed, lower frequency integrated circuits, or a combination thereof. These circuits typically have additional cost due to the cost of housing the separate components.

[0004] Over the years, specialized devices have been developed which lend themselves to a certain class or range of operation. Pseudomorphic high electron mobility transistor (pHEMT) devices are currently used for microwave and millimeter wave integrated circuit devices (MMIC) having extremely high performance. Frequencies typically range from X-band (8 GHz) to W-band (110 GHz) for such MMIC devices.

[0005] At least three different pHEMT devices are currently fabricated: enhancement mode pHEMT, depletion mode pHEMT, and power pHEMT.

SUMMARY

[0006] The present invention comprises an integrated circuit fabricated on a single substrate where the integrated circuit comprises devices comprising enhancement mode pHEMT, depletion mode pHEMT, and power pHEMT blocks, fabricated in a single process, wherein predetermined portions of the blocks may be interconnected to form a functional, operational electronic device.

[0007] The scope of protection is not limited by the summary of an exemplary embodiment set out above, but is only limited by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Fig. 1 is a schematic of an exemplary system;

[0009] Fig. 1a is an exemplary depletion mode circuit;

[0010] Fig. 1b is a set of tables indicating typical values for enhancement mode, depletion mode and power pHEMT devices;

[0011] Fig. 2 is an exemplary device comprising functional blocks;

[0012] Fig. 2a is an exemplary device comprising functional blocks and showing various exemplary inputs and outputs;

[0013] Fig. 3 is an exemplary enhancement mode pHEMT device;

[0014] Fig. 4 is an exemplary depletion or power mode pHEMT device;

[0015] Fig. 5a is an exemplary gain stage of an exemplary pHEMT device;

[0016] Fig. 5b is an exemplary 3 input "AND" cell of an exemplary pHEMT device;

[0017] Fig. 6 is a flowchart of an exemplary method of fabricating an operational integrated circuit according to the present invention; and

[0018] Fig. 7 is a flowchart of an exemplary fabrication process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0019] Referring now to Fig. 1, electronic device 10 comprises enhancement mode pHEMT 20, depletion mode pHEMT 30, and power pHEMT 40 fabricated onto a single substrate, e.g. 50.

[0020] Depletion mode pHEMT 30 may be single or multiple recess pHEMT 30. A typical circuit element using depletion mode pHEMT 30 is shown in Fig. 1a.

[0021] Typical values for enhancement mode 20, depletion mode 30 and power pHEMT 40 are shown in Fig. 1b.

[0022] Substrate 50 may be singly- or multi-layered and may comprise combinations of group III-V elements, e.g. GaAs, AlGaAs, InGaAs, InGaP, AlAs, and the like, or combinations thereof. In a preferred mode, substrate 50 comprises gallium arsenide.

[0023] Referring now to Fig. 2, an operational integrated circuit may be fabricated which contains a plurality of functional blocks 110,200,300,400 to form a useful, operational electronic device. Functional blocks, generally referred to by 200, 300, and 400, may comprise enhancement mode pHEMT blocks 200 comprising enhancement mode pHEMT 20 (shown in an exemplary layout in Fig. 3), depletion mode pHEMT blocks 300 comprising depletion mode pHEMT 30 (shown in an exemplary layout in Fig. 4), power pHEMT blocks 400 comprising power pHEMT 40. Other circuit blocks may be present as well, e.g. blocks 100. A plurality of blocks, e.g. integrated circuits, may therefore be present on a single substrate 50 (Fig. 1), at least one of the plurality of blocks 100,200,300,400 comprising enhancement mode pHEMT 20,

a further one of the plurality of blocks comprising depletion mode pHEMT 30, and yet a further one of the plurality of blocks comprising power pHEMT 40. Blocks 100,200,300,400 may be operatively interconnected, e.g. one or more devices and/or circuits in enhancement mode pHEMT block 200 may be operatively interconnected to one or more devices and/or circuits in depletion mode pHEMT block 300 and/or one or more devices and/or circuits in power pHEMT block 400 such as with conductive traces.

[0024] Functional blocks 200,300,400 may themselves comprise higher level functional logic, e.g. may comprise digital gates, serial shift registers, serial to parallel converters, parallel to serial converters, level shift registers, variable gain radio frequency (RF) amplifiers, variable RF phase shifters, variable RF attenuators, resistors, inductors, capacitors, and the like, or combinations thereof.

[0025] For example, referring additionally to **Fig. 2a**, analog inputs 52 may be fabricated and interconnected with at least one of enhancement mode pHEMT block 200, depletion mode pHEMT block 300, power pHEMT block 400, circuit block 110, or a combination thereof. Circuit block 110 may further comprise clock input 56 in communication with at least one of enhancement mode pHEMT block 200, depletion mode pHEMT block 300, power pHEMT block 400, or a combination thereof. Digital input 54 may be further fabricated to be in communication with at least one of enhancement mode pHEMT block 200, depletion mode pHEMT block 300, power pHEMT block 400, or a combination thereof. One or more outputs of the functional circuitry may be fabricated as well, e.g. radio frequency output 58.

[0026] Referring back to **Fig. 2**, when fabricated, functional blocks 110,200,300,400 may then be interconnected to form an active or passive electronic device, e.g. an analog to digital converter or a microwave and millimeter wave integrated circuit (MMIC). Devices

fabricated according to the present invention comprise an operational circuit, i.e. active or passive electronic devices, capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies.

[0027] Referring additionally to **Fig. 3** and **Fig. 4**, each functional block 200,300,400 may comprise one or more active devices, e.g. as shown in **Fig. 3** enhancement mode pHEMT block 200 may comprise a plurality of enhancement mode pHEMT devices 20. As shown in **Fig. 4**, depletion mode pHEMT block 300 may comprise a plurality of depletion mode pHEMT devices 30. In a preferred embodiment, power mode pHEMT block 400 may be laid out similarly to depletion mode pHEMT block 300.

[0028] Additional elements consisting of resistors, capacitors and inductors may be included in all blocks. Referring additionally to **Fig. 7**, resistor, capacitor and inductor contacts may be formed, at step 618. A nitride layer may be formed, step 620, to form a capacitor dielectric as well as an inductor spacer. A top contact may be formed, at step 622 Metal 1. Resistors may be formed, e.g. at step 616.

[0029] **Fig. 5a** illustrates an exemplary gain stage of an exemplary pHEMT device 10. **Fig. 5b** illustrates an exemplary three input AND cell of an exemplary pHEMT device 10.

[0030] **In the operation of an exemplary embodiment**, referring now to **Fig. 6** and **Fig. 2**, in a preferred embodiment, electronic device 10 (**Fig. 2**) may be created in a single fabrication process to form one or more functional blocks 100,200,300,400 (**Fig. 2**) where functional blocks 100,200,300,400 can be combined to create an operational device, e.g. device 10. An operational integrated circuit 10 may be fabricated according to the present invention in a single fabrication process by creating, at step 500, first block 200 comprising a pHEMT enhancement mode transistor 20 on substrate 50; using the same fabrication processing,

creating, at step 502, second block 300 comprising a pHEMT depletion mode transistor 30 on substrate 50, where second block 300 is operatively connected to first block 200; and, using the same fabrication processing, creating, at step 504, third block 400 comprising a power pHEMT transistor 30 on substrate 50, third block 400 operatively connected to at least one of first block 200 and second block 300. Additional functional blocks 100 may be fabricated in the same fabrication process. The order in which blocks 100,200,300,400 are created is not material.

[0031] In a currently preferred embodiment, logic circuitry design utilizes a four μm spacing for all interconnects. For depletion mode pHEMT 30, a single recess is preferred where V_p = one tenth of a volt (0.1v). For enhancement mode pHEMT 20, a single recess is also preferred where V_p = a negative one volt (-1v). For power pHEMT 30, a double recess is preferred where V_p = a negative one volt (-1v).

[0032] Referring now to **Fig. 6** and **Fig. 1**, in a preferred embodiment a triple etch-stop process is employed in fabricating device 10 (**Fig. 1**), e.g. to create wide recess, e-mode, and d-mode gates. An ohmic layer may be created, 600, on substrate 50 (**Fig. 1**) and devices 20,30,40 (**Fig. 1**) isolated, at step 602. A typical recess is illustrated at 40 in **Fig. 1**, and a wide recess, 604, illustrated at 20 in **Fig. 1**. Thickness of layers, e.g. 60,61,62 (**Fig. 1**) may be fine tuned to meet pinch-off voltage specifications.

[0033] A first T-gate, as that term is understood by those of ordinary skill in the art, may then be fabricated, step 606, typically for all devices to be fabricated according to the present invention. Gate recess and metal may be fabricated, 608. Optionally, a second T-gate pass, 610, and gate recess and metal, 612, may be fabricated.

[0034] Additional elements consisting of resistors, capacitors and inductors may be included in all blocks. Additional layers may be fabricated on substrate 50, step 614, and

various additional devices fabricated, e.g. resistors at step 616. These additional layers may be created on substrate 50 to form resistors, capacitors, and inductors, e.g. steps 616-622. Referring still to Fig. 6, resistor, capacitor and inductor contacts may be formed, at step 618. A nitride layer may be formed, step 620, to form a capacitor dielectric as well as an inductor spacer. A top contact may be formed, at step 622 Metal 1. Resistors may be formed, e.g. at step 616.

[0035] An MIM top metal layer may be created, 626 followed by an air bridge metal layer, 628, and a protective overcoat, 630. Various finishing operations may then be accomplished, e.g. steps 634-642.

[0036] Using the present inventions method of fabrication, one watt power amplifiers, small signal monolithic microwave and millimeter wave integrated circuits (MMICs), and control circuits may be integrated on a single substrate such as substrate 50 (Fig. 1). One such device 10 may be an analog to digital converter (A/DC) capable of operating a X-band frequencies, e.g. up to 10 GHz. However, as will be appreciated by those in the art, functional blocks 100,200,300,400 may be combined in numerous ways to form numerous circuits, e.g. devices 10 combining digital, radio frequency (RF), and power functional blocks 100,200,300,400 on common substrate 50. Moreover, A/DC devices 10 could be integrated into an even higher function device 10, e.g. one that may be used to replace heterodyne receiver technology and have complete integration of RF to Receiver I and Q data on one chip, e.g. a receiver on a chip.

[0037] It will be understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated above in order to explain

the nature of this invention may be made by those skilled in the art without departing from the principle and scope of the invention as recited in the following claims.